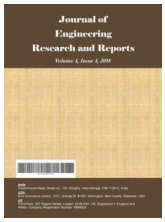

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Design of Common-gate with Common-source Active Balun for WiMAX Receiver Front-end

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Authors' contributions

This work was carried out in collaboration amongst the authors. All authors read, reviewed and approved the final manuscript.

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ABSTRACT

This paper presents a design and simulation study of a common-gate with common-source active balun circuit implemented in a standard 90-nm complementary metal-oxide semiconductor (CMOS) process. The active balun design is intended for worldwide interoperability for microwave access (WiMAX) application, with operating frequency of 5.8 GHz and supply voltage of 1 V. Measurements are taken for parameters namely gain difference, phase difference, and noise figure. The common-source active balun design achieved a minimal gain difference of 0.04 dB, phase difference of 180 ± 1.5 degrees, and noise figure of 8.76 dB, which are comparable to past active balun designs and researches. The design eventually achieved a low power consumption of 4.45 mW.

Keywords: Common-gate with common-source active balun; gain difference; phase difference; WiMAX.

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1. INTRODUCTION

The radio frequency (RF) front-end of a wireless receiver is one critical part in many wireless communication systems such as bluetooth, wireless fidelity (WiFi), and worldwide interoperability for microwave access (WiMAX). A typical wireless receiver is shown in Fig. 1 diagram.

Some key RF front-end circuits are often designed in differential configuration. Fully-differential approach is mostly preferred in RF integrated circuit (RFIC) design due to its advantages, particularly the high immunity to common-mode noises, rejection to parasitic couplings, and increased dynamic range [1-2]. In order to supply input signal to differential circuits, a building block capable of supplying balanced differential signals is needed without sacrificing the performance of the overall system in terms of gain, noise figure, and linearity. Active balun (balanced-unbalanced) is capable to perform the necessary tasks.

A balun circuit is a type of transformer that converts signals that are single-ended or unbalanced with respect to ground into signals that are differential or balanced with respect to ground, and vice versa. Baluns can be classified as either active or passive baluns depending on the devices used. Active baluns, although unidirectional and more complex to implement, are preferred over their passive counterparts because they can produce gain, occupy less chip area and can operate at higher frequencies [1-3].

Active balun circuit can be used as the first block of the WiMAX receiver front-end to supply differential signal to a differential low-noise amplifier (LNA). It can also be used to supply differential signal to a mixer. Fig. 2 shows the active balun circuit as an intermediate block between the LNA and the mixer. Note that the configuration depends on the gain, noise figure (NF), and linearity requirements of the system. Since LNA is the first block in the receiver front end, it is critically designed with high gain of at least 25 dB and noise figure of less than 2 dB. Based on past researches, active balun has relatively high noise figure and lower gain performance compared to LNA, hence cannot be considered as the first block in the receiver front-end. Finally, the challenge is to design an active balun as an intermediate block to allow the LNA's output to connect with a differential mixer's input, with performance conforming to the requirement for the WiMAX receiver front-end.

2. ACTIVE BALUN DESIGN

In this research paper, a differential active balun is designed and implemented in a standard 90-nm complementary metal-oxide semiconductor (CMOS) technology. The supply voltage (V_{DD}) for the design is set to 1 V. The lengths (L) of all transistors are set to 100 nm, which is the minimum allowed channel length for the technology used. Transistor widths (W) are carefully computed to ensure the operation of all the transistors at saturation. As mentioned earlier, the paper deals with the design of active baluns as intermediate block between LNA and mixer in the WiMAX receiver front-end. Table 1 summarizes the target specifications of the active balun design. These values are based from past active balun researches [1-4] and from the summary of parameters as per WiMAX standard [5].

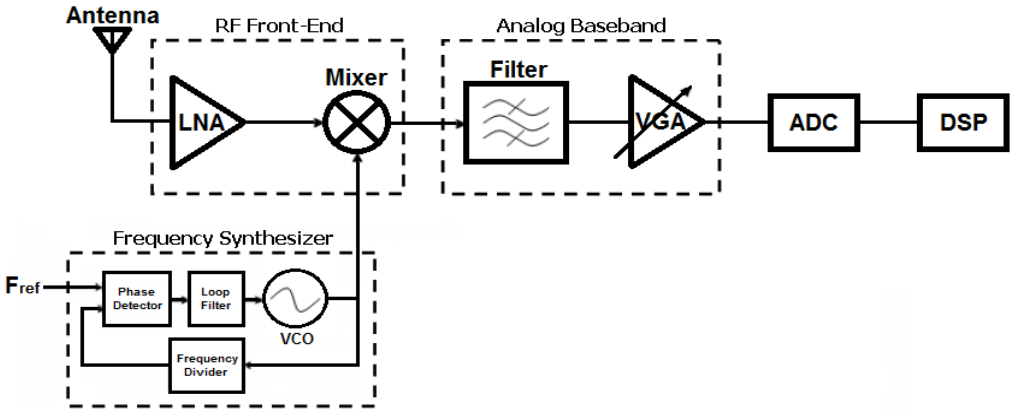

Fig. 1. Block diagram of a wireless receiver

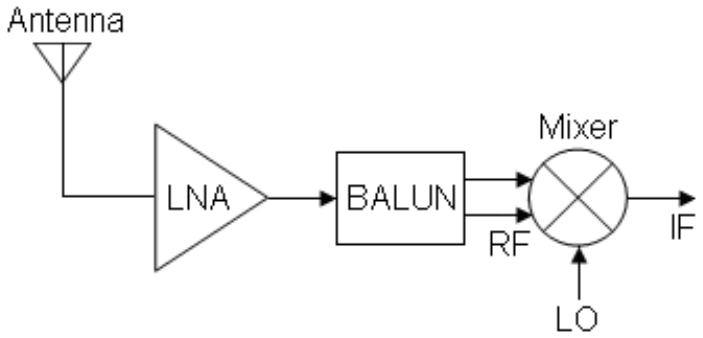

Fig. 2. Active balun as intermediate block between LNA and mixer

Table 1. Minimum target parameter values for the differential active balun design

Parameters	Value
Frequency	5.8 GHz
Gain difference	< 1 dB
Phase difference	180 ± 10 degrees
Noise figure	< 10 dB
Power consumption	< 10 mW

Two most important parameters of the active balun are the gain difference and phase difference. Gain difference is the difference of the gains from the two output nodes of the active balun while the phase difference is the difference between the phase of the non-inverting output node (RFout1) and the phase of inverting output node (RFout2) of the active balun. Noise figure on the other hand, is the measure of the amount signal-to-noise-ratio (SNR) degradation introduced by the circuit as seen in the output.

The common-gate with common-source active balun in Fig. 3 is comprised of 2 amplifiers namely common-gate amplifier M1 in the 1st stage and common-source amplifier M2 in the 2nd stage. The input signal is fed into the drain of M1 and into the gate of M2, while the outputs are probed at the drains of M1 and M2. Load resistors R1 and R2 dictate the output voltages as well as the voltage gains of the two output signals with respect to the input signal.

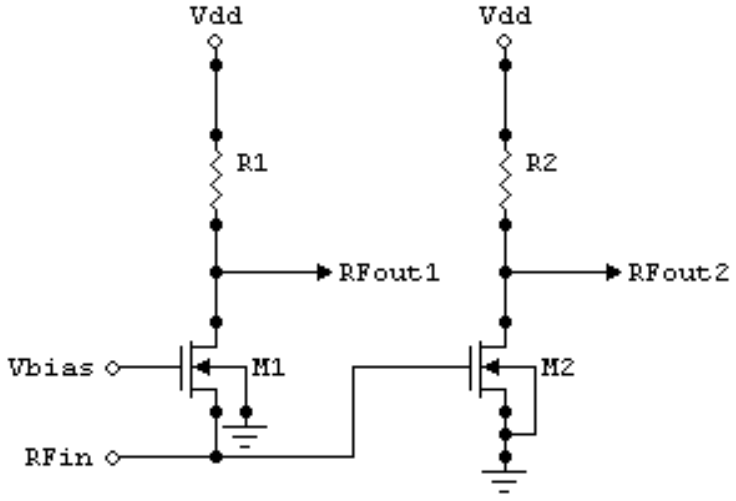

Fig. 3. Schematic diagram of common-gate with common-source active balun

Common-source topology exhibits a relatively high input impedance while providing voltage gain and requiring a minimal voltage headroom. With this, it finds wide application in analog circuits and its frequency response is of interest. Common-gate topology exhibits no Miller multiplication of capacitances, potentially achieving a wide band [6-7]. However, the low input impedance may load the preceding stage. Moreover, since the voltage drop across R1 is typically maximized to obtain the required gain, the DC (direct current) level of the input signal must be quite low. With the two topologies connected as such to function as an active balun, one major challenge would be to generate balanced gain for the two outputs RFout1 and RFout2 with respect to the input signal RFin, given that the input signal is fed into two different transistor ports.

To achieve the maximum output swing for M2, VRFout2 (or just V2) should be between supply voltage (V_{DD}) and the V_{DSAT} or the overdrive voltage (V_{OV}) of the transistor, ensuring also that the transistor operates at the saturation region. With V_{DD} = 1 V, and V_{OV} set to 200 mV, the output at RFout2 could swing from 0.2 V to 1 V. With the said output swing range, output DC voltage (or bias voltage) V2 is computed in Eq. (1) to (2).

$$V_{DD} > V2 \geq V_{DSAT2} \quad \rightarrow \quad 1\,V > V2 \geq 0.2\,V \tag{1}$$

$$V2 = V_{RFout2} = \frac{V_{DD} + V_{OV2}}{2} = \frac{1\,V + 0.2\,V}{2} = 0.6\,V \tag{2}$$

Input bias voltage V_{RFin} (or simply V_{IN}) is the same as the gate voltage (V_{G2}) of M2 and the source voltage (V_{S1}) of M1. To satisfy the $V_{DS2} \geq V_{DSAT2} = V_{OV2}$, input voltage ($V_{IN}$) should be properly set. With threshold voltage (V_t) set to 400 mV,

$$V_{DS2} = V_{GS2} - V_t \geq V_{DSAT2} \quad \rightarrow \quad (V_{IN} - 0) - 0.4V = 0.2\,V \tag{3}$$

$$V_{IN} = 0.6\,V \tag{4}$$

With V_{IN} as the source voltage (V_{S1}) of transistor M1, output DC voltage for RFout1 which is V1 (or V_{RFout1}) could be calculated for maximum output swing.

$$V_{DD} > V1 \geq V_{IN} \quad \rightarrow \quad 1\,V > V1 \geq 0.6\,V \tag{5}$$

$$V1 = V_{RFout1} = \frac{V_{DD} + V_{IN}}{2} = \frac{1\,V + 0.6\,V}{2} = 0.8\,V \tag{6}$$

Maximum output swing could be achieved at output DC voltage V1 set to 0.8 V and at V2 set to 0.6 V. To compute for the proper biasing of transistor M2, with input voltage kept at minimum allowed which is at 0.6 V,

$$V_{DS1} = V_{GS1} - V_t \geq V_{DSAT1} \quad \rightarrow \quad (V_{BIAS} - V_{IN}) - 0.4\,V = 0.2\,V \tag{7}$$

$$V_{BIAS} = 1.2\,V \tag{8}$$

If overdrive voltage V_{OV} is set to 100 mV for both transistors M1 and M2, output swings for V1 and V2 could be adjusted. Also, V_{IN} and bias voltage (V_{BIAS}) for M2 could be lowered. Recalculations are shown in Eq. (9) to (12).

$$V2 = \frac{V_{DD} + V_{OV2}}{2} = \frac{1\,V + 0.1\,V}{2} = 0.55\,V \tag{9}$$

$$V_{IN} = 0.4\,V + 0.1\,V = 0.5\,V \tag{10}$$

$$V1 = \frac{V_{DD} + V_{IN}}{2} = \frac{1\,V + 0.5\,V}{2} = 0.75\,V \tag{11}$$

$$V_{BIAS} = V_{IN} + 0.4\,V + 0.1\,V = 1\,V \tag{12}$$

With input DC (or bias) voltage (V_{IN}) set to 0.5 V, gmoverId could be derived for the two branches or outputs.

$$g_{m1} = \frac{\delta I_{DS1}}{\delta V_{GS1}} = \mu C_{ox} \frac{W_1}{L_1} (V_{GS1} - V_t)(1 + \lambda V_{DS1}) \tag{13}$$

$$g_{m2} = \frac{\delta I_{DS2}}{\delta V_{GS2}} = \mu C_{ox} \frac{W_2}{L_2} (V_{GS2} - V_t)(1 + \lambda V_{DS2}) \tag{14}$$

Substituting the expression for the drain current (I_{DS}) of into g_m expressions,

$$g_{m1} = \frac{\delta I_{DS1}}{\delta V_{GS1}} = \frac{2I_{DS1}}{V_{GS1} - V_t} = \frac{2I_{DS1}}{V_{BIAS} - V_{IN} - V_t} \tag{15}$$

$$\frac{g_{m1}}{I_{DS1}} = \frac{2}{V_{BIAS} - V_{IN} - V_t} = gmoverId1 \tag{16}$$

$$g_{m2} = \frac{\delta I_{DS2}}{\delta V_{GS2}} = \frac{2I_{DS2}}{V_{GS2} - V_t} = \frac{2I_{DS2}}{V_{IN} - V_t} \tag{17}$$

$$\frac{g_{m2}}{I_{DS2}} = \frac{2}{V_{IN} - V_t} = gmoverId2 \tag{18}$$

For low power design, higher gmoverId is recommended. To achieve such, V_{IN} and V_{BIAS} should be optimized. With V_{BIAS} fixed, increasing the V_{IN} increases the efficiency of M1 in terms of gmoverId1. On the other hand, increasing V_{IN} would decrease the efficiency of M2 in terms of gmoverId1. Lowering the drain current or supply current (I_{DS}) would also mean lowering g_m to maintain the efficiency for low power consumption. With this, there is a limit in the effectiveness of optimizing the input voltage (V_{IN}), bias voltage (V_{BIAS}) and supply current (I_{DS}) to maximize the efficiency in terms of gmoverId.

Furthermore, the design is optimized to meet the target performance specifications suitable for WIMAX receiver, and is implemented in a standard 90-nm CMOS process using Cadence Virtuoso software [8], computer-aided design (CAD) tool and an electronic design automation (EDA) software tool. Table 2 summarized the common-gate with common-source active balun parameters.

3. RESULTS AND DISCUSSION

The common-gate with common-source active balun is characterized and designed to achieve the target specifications. The extraction of all device parameters for use in simulations is done using Synopsys Star-RCXT [9]. Simulations of the extracted view are done using Cadence Design Systems software. The active balun is designed to operate at 5.8 GHz, which is a typical frequency for WiMAX applications. Measurements in the simulation plots are taken at 5.8 GHz.

3.1 Gain and Gain Difference

There are many types of power gain defined for an amplifier, with the most commonly specified and often the most useful – the transducer gain, G_T. It is defined as the ratio of the power delivered to the load to the power available from the source. Gain difference or gain error is the difference of the gains from the two output nodes of the active balun, and is considered as one of the most important parameters of the active balun design. Ideally, the gain difference of an active balun should be zero in magnitude. The responses in Figs. 4 and 5 for the gain and gain difference, respectively, are determined using AC (alternating current) analysis. Input bias voltage is set at 0.45 V. Both transistors M1 and M2 satisfied the requirements for saturation region condition.

Common-gate with common-source active balun is designed to achieve a gain of just above 0dB. This is validated in the AC gain results in Fig. 4. Gain difference in Fig. 5 is expected to be close to zero since the gain response for the two outputs is very close to each other.

3.2 Phase and Phase Difference

Another important parameter of an active balun is the phase difference. Phase difference is the difference between the phase of the non-inverting output node and the phase of inverting output node of the active balun. Figs. 6 and 7 show the AC analysis phase and phase difference responses, with ideal input voltage source.

The results are within the target specification for the phase difference. AC analysis measurement for phase difference is at 178.5 degrees at 5.8 GHz frequency of operation.

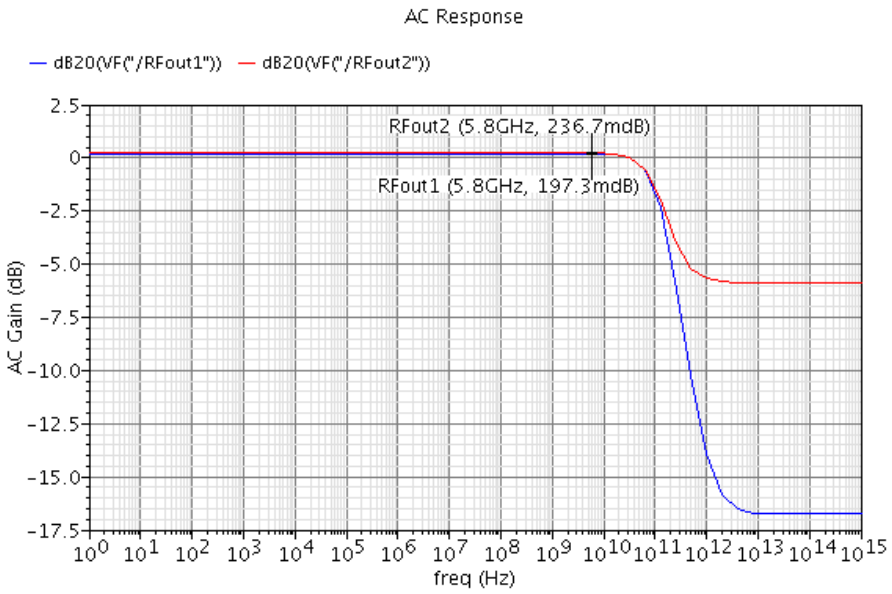

Fig. 4. Gain plot using AC analysis

Table 2. Common-gate with common-source active balun parameters and expressions

Parameters	Value
Input bias voltage	0.5 V
Output DC voltage for maximum swing	0.75 V (RFout1), 0.55 V (RFout2)
Input impedance	$1 / (g_{m1} + g_{mb1})$
Output impedance, with resistor and capacitor loads	R1 || 1/*s*C1 (RFout1), R2 || 1/*s*C2 (RFout2)
Voltage gain, simplified (*s* = 0)	$\frac{(g_{m1}+g_{mb1})R1}{1+(g_{m1}+g_{mb1})Rs}$ (RFout1) $-g_{m2}R2$ (RFout2)
Output noise voltage	$\frac{k_BT}{C1}[1+\gamma(g_{m1}+g_{mb1})R1]$ (RFout1) $\frac{k_BT}{C2}(1+\gamma g_{m2}R2)$ (RFout2)
Noise figure	$10log\left[1+\frac{1+\gamma(g_{m1}+g_{mb1})R1}{C1\cdot 4\frac{1+\gamma g_{m1}R1}{(g_{m1}+g_{mb1})^2R1}A_{v1}}\right]$ (RFout1) $10log\left[1+\frac{1+\gamma g_{m2}R2}{C2\cdot 4\frac{1+\gamma g_{m1}R1}{(g_{m1}+g_{mb1})^2R1}A_{v2}}\right]$ (RFout2)

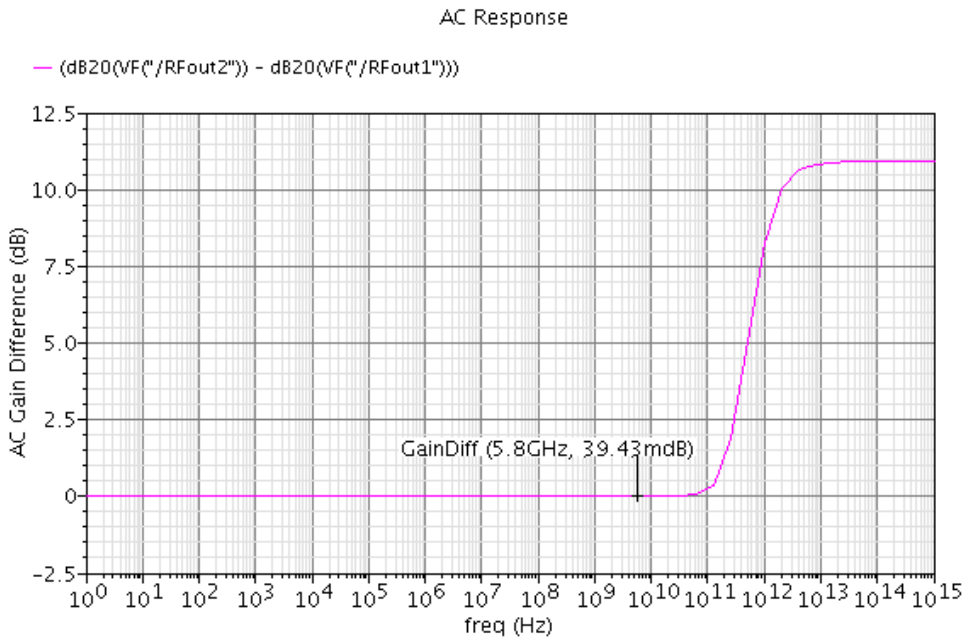

Fig. 5. Gain difference plot using AC analysis

3.3 Noise Figure

Noise performance is an important design consideration since it determines the susceptibility of the active balun to unwanted signal or noise [2,10]. One important design parameters is the noise figure, which is a measure of the amount of signal-to-noise-ratio degradation introduced by the circuit as seen at the output. Fig. 8 shows the noise figure result using PSS+PNoise analysis.

Noise figure of 7.199 dB and 8.762 dB for RFout1 and RFout2 with respect to RFin are generated using PSS+PNoise analysis [11] taken at frequency of 5.8 GHz. The values conformed to the noise figure requirement set for the active balun design.

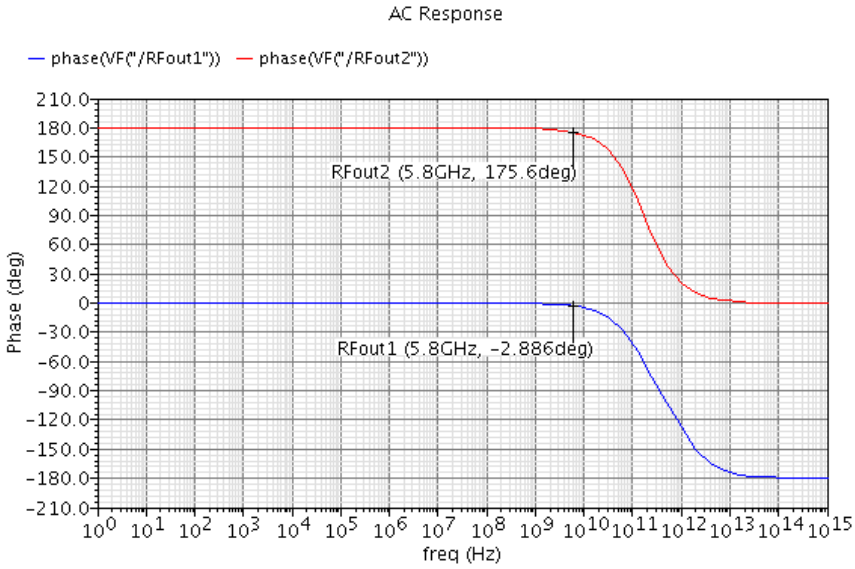

Fig. 6. Phase plot using AC analysis

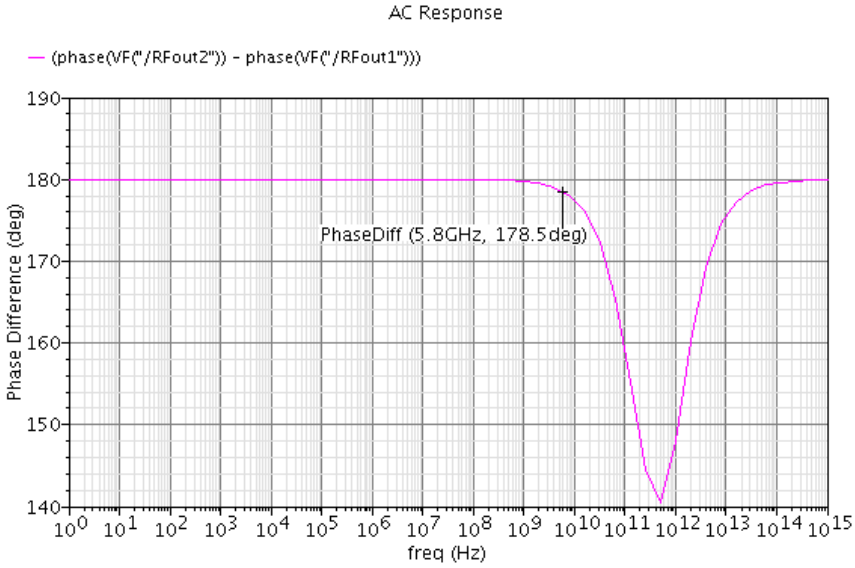

Fig. 7. Phase difference plot using AC analysis

Table 3. Performance summary of differential active balun

Parameters	Value	Target
Process/Technology	90-nm CMOS	90-nm CMOS
Supply voltage	1 V	1 V
Frequency	5.8 GHz	5.8 GHz
Gain difference	0.040 dB	< 1 dB
Phase difference	178.5 degrees	180 ± 10 degrees
Noise figure	7.199 dB (RFout1), 8.762 dB (RFout2)	< 10 dB
Power consumption	4.449 mW	< 10 mW

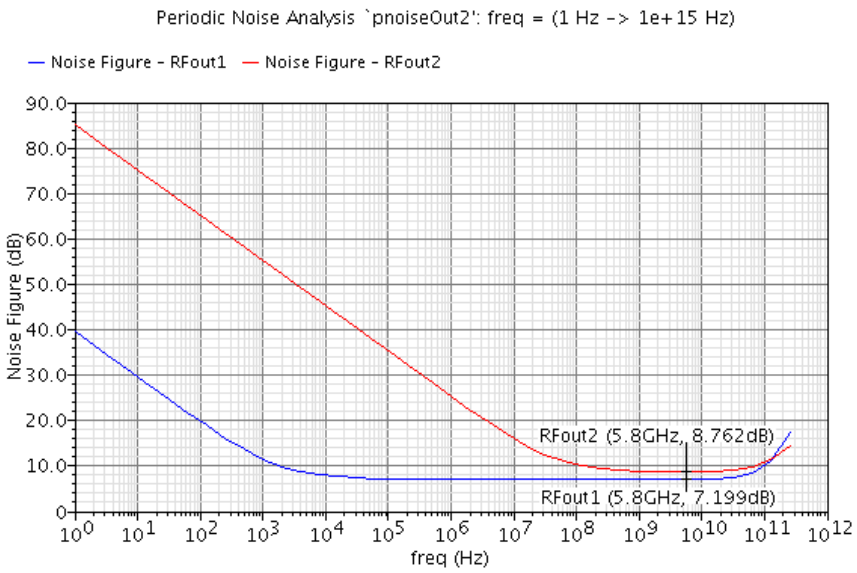

Fig. 8. Noise figure plot

3.4 Results Summary

Table 3 summarizes the performance of the three active balun designs.

The common-gate with common-source active balun design achieved a gain difference better than 1 dB and a phase difference of 180 ± 10 degrees or better at frequency of 5.8 GHz. The balun is affected with the input and output loading since the circuit is designed with ideal input voltage source and no termination ports included. Low power consumption of at most 4.45 mW is achieved, comparable to other low power designs in the past researches.

4. CONCLUSION AND RECOMMENDATIONS

A common-gate with common-source active balun is designed and implemented in a standard 90-nm CMOS process, and carefully designed to satisfy the WiMAX receiver requirement at 5.8 GHz. Simulation measurements are taken for parameters such as gain, phase, gain difference, phase difference, and noise figure.

The design achieved gain difference of 0.04 dB and phase difference of 180 ± 1.5 degrees. Noise figure performance is at around 7.2–8.76 dB, comparable to previous designs and researches. Low power consumption of at most. 4.45 mW is achieved, comparable to other low power designs.

Future work and research could explore designing active balun with high gain. Although it will sacrifice the bandwidth, it can still be realized at lower frequencies for practical applications. One possible work would be to integrate the active balun functionality on the circuit design of a differential circuit like that of the double-balanced mixer or differential LNA.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

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