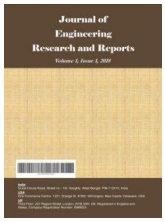

Journal of Engineering Research and Reports

6(1): 1-6, 2019; Article no.JERR.49689

A Study of Vacuum Efficiency for Silicon on Insulator Wafers

Bryan Christian S. Bacquian[1] and Frederick Ray I. Gomez[1*]

[1]STMicroelectronics, Inc., Calamba City, Laguna, 4027, Philippines.

Authors' contributions

This work was carried out in collaboration between both authors. Both authors read and approved the final manuscript.

Article Information

DOI: 10.9734/JERR/2019/v6i116936
Editor(s):
(1) Dr. David Armando Contreras-Solorio, Professor, Academic Unit of Physics, Autonomous University of Zacatecas, Mexico.
Reviewers:
(1) Yuan-Tsung Chen, National Yunlin University of Science and Technology, Taiwan.
(2) A. Ayeshamariam, Khadir Mohideen College, India.
(3) Snehadri Ota, Institute of Physics, India.
Complete Peer review History: http://www.sdiarticle3.com/review-history/49689

Original Research Article

Received 03 April 2019
Accepted 17 June 2019
Published 24 June 2019

ABSTRACT

The development on thinner packages has become the trend and focus in semiconductor packaging industry. The necessity of thinner packages also entails a thinner vertical structure of the integrated circuit (IC) design. As a major contributor on the vertical structure of the IC package, die or wafer is also essential to go thinner. As the wafer goes thinner, various problems may occur during transport and even the back grinding process, itself.

Wafer warpage is one of the main concerns during the process. The effect of proper vacuuming will play major role in processing SOI wafers. Insufficient vacuum may cause non-planar wafer in contact with the chuck table that may result to poorer grinding and worst broken wafer.

Different silicon wafer technology has been released to cater different functionality on different industry markets. One popular silicon technology is Silicon On Insulator (SOI) technology. SOI wafers have a step type passivation wherein the edge of the wafer is observed to have 30um thinner than its center. The stepping effect also contributes to the 0.5mm wafer warpage prior back grinding. Evaluating the effect of vacuum efficiency to eliminate such warpage is discussed on this technical paper.

Keywords: Wafer preparation; silicon on insulator; SOI wafer; vacuum.

**Corresponding author: Email: frederick-ray.gomez@st.com;*

1. INTRODUCTION

Achieving the package requirements of a semiconductor integrated circuit (IC) device would mean attaining a thinner die during the back end process. The major process brick responsible for grinding the silicon die to its thickness is wafer back grinding. As a major preliminary process at the back end, one of its sub processes is the wafer preparation prior grinding wherein silicon wafer is been taped on the active layer to protect it from any contaminants and water penetration during the grinding process. At the main back grinding process, firstly, wafer is vacuumed on a chuck table to ensure wafer flatness. Wafer should be properly stuck down to ensure or eliminate leakage that may cause flatness issue and will theoretically generate uneven grinding. However, original equipment manufacturers (OEM) have different designs of chuck tables in terms of porous area wherein vacuum are applied. The study will discuss the importance of vacuum efficiency during the process.

1.1 Silicon on Insulator Wafer

Silicon on Insulator (SOI) wafer technology refers to the use of a layered silicon-insulator-silicon substrate, to reduce parasitic capacitance and thereby improving performance [1-2]. The implementation of SOI technology is one of several manufacturing strategies employed to allow the continued miniaturization of microelectronics colloquially referred to as extending Moore's law [2-3]. SOI process has been developed so as to be used for RF applications [4]. The inclusion of enhanced sapphire substrate allows the complementary metal-oxide semiconductor (CMOS) node to have a high isolation, high linearity, and electrostatic discharge (ESD) tolerance. The glass passivation on the wafer's top layer creates a stepping effect on the edge of the wafer in Fig. 1.

Fig. 1. Wafer edge structure

In line with the stepping effect, SOI wafers are measured prior wafer taping and observed to have the edge area 30 µm thinner than the device area as depicted in Fig. 2. Also, the wafers after having taped are observed to have a warpage in Fig. 3 of 0.5 mm around the edge area.

1.2 Chuck Table Design

Chuck table plays a major role of ensuring wafer flatness during wafer backgrinding. Wafer flatness would be dependent on the amount of wafer clamp vacuum pressure and helps compensate wafer warpage during wafer. Normally, the vacuum source pressure must be identical to wafer clamp vacuum, if not, vacuum leakage will be experienced.

Chuck table varies between different wafer backgrinding OEMs. Specifically, chuck table differs on the area wherein vacuum is applied. Chuck table has a porous design wherein vacuum will be effectively distributed on the given area.

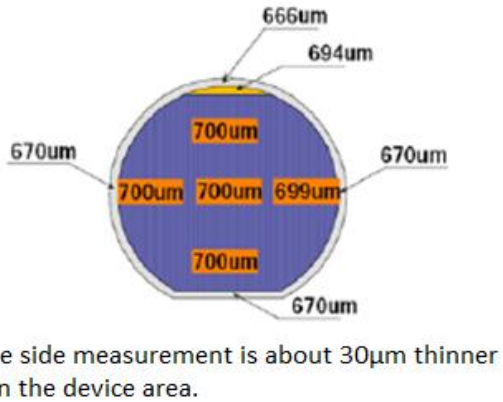

Fig. 2. Wafer thickness prior taping

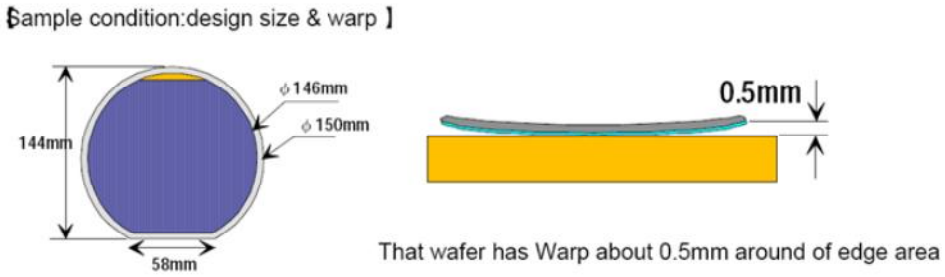

Fig. 3. Wafer warpage after taping

2. LITERATURE REVIEW

2.1 Wafer Warpage

As the electronics device goes thinner, the trend of IC packaging also goes thinner. The requirement of thinner wafers is also being developed. One major problem is the wafer warpage that make incur breakage during transport but the reduction will further improve the process window of handling thin wafer. It is worth noting that subsequent assembly and test process flow also adapts with the development and trend on wafer technology [5-7].

Vacuum efficiency acts as the major contributor of reducing or even eliminating wafer breakage during the automatic backgrinding. Two parts of the system that will require higher vacuum efficiency are the robot arm and chuck table. Low vacuum at robot arm will lead to errors during transport or worse, wafer breakage. However, low vacuum at the chuck table will cause inferior grinding.

2.2 Wafer Warpage Mechanism

A common wafer mechanism is a normal warpage [8] illustrated in Fig. 4. This is generally caused by the natural stress created by mechanical backgrinding. The proportional relationship of wafer warpage and mechanical stress states that when the final thickness decrease this probably caused by high mechanical stress that may lead to high wafer warpage.

2.3 Mechanical Stress after Wafer

Stresses applied during encapsulation may crack the die and cause other stress-related failures. Optimized wafer strength is needed to ensure reliability during both fabrication and packaging. However, grinding anything inevitably leaves flaws on its surface, which can weaken both the wafer and the individual dice sawn from it. Given thermal or mechanical stress, these flaws may then spread into active regions, and may crack the die.

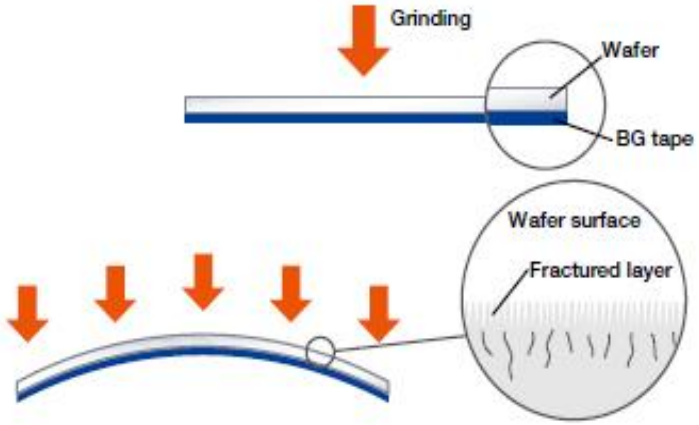

Fig. 4. Normal warpage

After backgrinding, the wafer will exhibit a scratch pattern on the backside as shown in Fig. 5. These scratch patterns and the depth of the scratches on the surface of the wafer are directly proportional to the size of the grit and the pressure exerted on the wafer during the grinding process. The depth of the scratches and the backside surface roughness of the semiconductor die have a direct correlation to the strength of the die, so it is critical that the finished backside surface of the wafer be as smooth (or polished) as possible [9].

3. EXPERIMENTATION

3.1 Machine Configuration Evaluation

SOI wafers, on a 6" diameter outline, have been used to evaluate the capability of two different wafer backgrinding OEMs. Wafer warpage was also noticeable prior loading to both evaluation machines. The two different OEMs have difference on the chuck table, wherein OEM 1 has a smaller porous area compared to OEM 2 by 13 µm in Fig. 6. The porous area of OEM 2 is also observed to be on the same diameter compared to OEM 1.

4. RESULTS AND DISCUSSION

Two different chuck tables have different responses on the efficiency of the vacuum during wafer handling prior backgrinding. OEM 2 with the big diameter of the porous area on the chuck table with 147 mm cannot handle the step type passivation of the SOI wafer. Clamping error was encountered due to low vacuum efficiency of 80% on the OEM 2 chuck table. Full auto mode is also cannot be performed caused by low vacuum pressure that is not enough to handle the wafer before backgrinding.

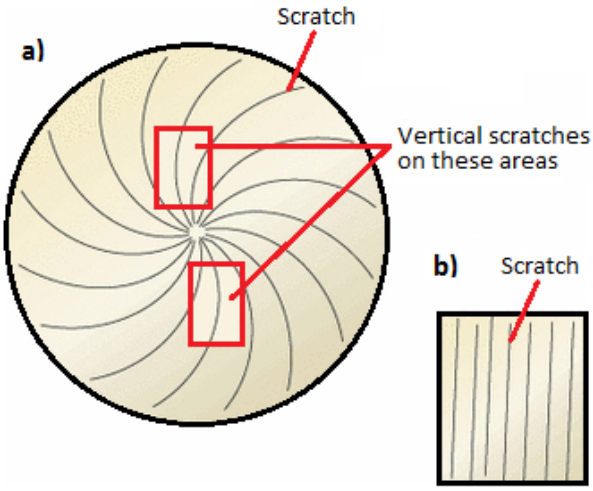

Fig. 5. Vertical scratches after wafer

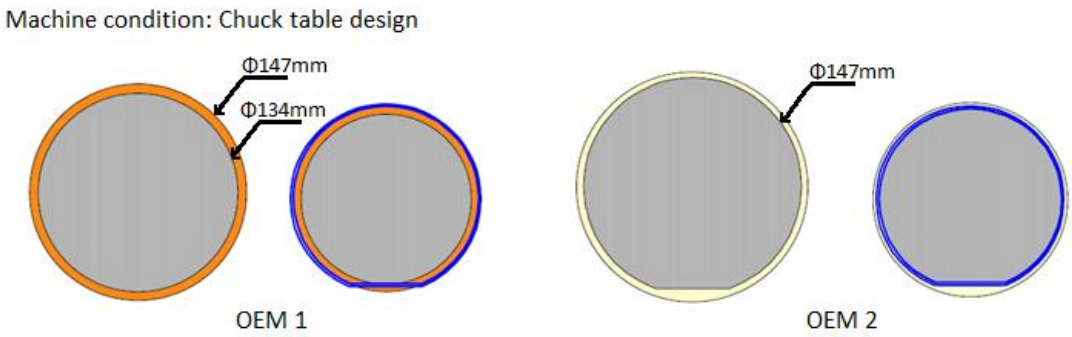

Fig. 6. Chuck table design

OEM 1 with a smaller porous area exhibits a 95-100% vacuum efficiency. SOI wafer are properly seated on the chuck table therefore ensuring no leakage is encountered on between surface contacts of the wafer. Full auto mode is also enabled and then preceded to auto backgrinding process. However, during the unloading of the finished wafer, vacuum errors occurred in Fig. 7 due to higher wafer warpage after backgrinding. There is a manifestation of vacuum leakage due to extreme wafer warpage. Afterwards, manual intervention is also cannot be performed due to vacuum leakage and that leads to manual unloading of the wafer on the robot arm.

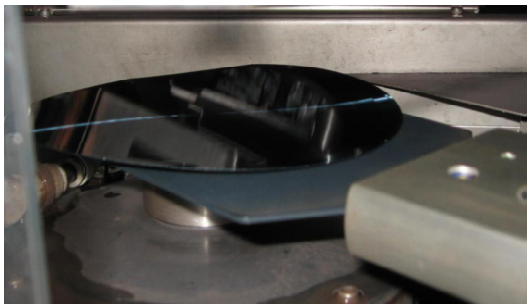

Fig. 7. Vacuum error on the robot arm

Back side image of the wafer has also been inspected using high magnification microscope as shown in Fig. 8. Uneven surface was observed at the edge of the wafer, which can also be considered a potential cause of broken wafer during process of transporting wafer from one station to another at pre-assembly. Also, the occurrence of uneven surface at the back of the wafer also coincide with the step at the edge of the wafers.

Fig. 8. Back side image of the SOI wafer

5. CONCLUSION AND RECOMMENDATIONS

Chuck table design is important in handling special wafer surface design. Vacuum efficiency should be properly studied to ensure no leakage on the chuck table during the grinding process. However, the smaller porous size of the chuck table caused the uneven surface at the back side of the wafer due to no vacuum holding the overhang structure on the edge of the wafer.

Based on the results, it is highly recommended to use high vacuum efficient chuck table to properly handle incoming wafer warpage and ensure good flattening on the chuck table and eliminating the possibility of inferior grinding. Redesign of special robot arms should also be considered to eliminate the possibility of wafer breakage when handling or unloading thinner wafers after grinding or use an inline BG-mount system. Moreover, a special process should be considered wherein making an outer circumference lip, where no grinding pressure is applied on the edge of the wafer during backgrinding. For subsequent critical processes like that of the wafer saw, discussions presented in [10] are helpful to mitigate defects related to wafer preparation. It is also important that the assembly manufacturing processes ensure proper ESD checks and controls. Discussions cited in [11] are helpful to realize ESD-related controls.

ACKNOWLEDGEMENTS

The authors would like to express sincerest appreciation to the Central Engineering and Development – New Product Introduction (NPI) team and colleagues of STMicroelectronics Calamba who have greatly contributed to the success of the work. The authors are grateful to the Management Team for the extensive support.

COMPETING INTERESTS

Authors have declared that no competing interests exist.

REFERENCES

1. Celler GK, Cristoloveanu S. Frontiers of silicon-on-insulator; 2003.
2. Wosinski L, Wang Z, Tang Y. Interfacing of silicon-on-insulator nanophotonic circuits to the real world. 12th International Conference on Transparent Optical Networks; 2010.
3. Mendez H. Silicon-on-insulator - SOI technology and ecosystem - Emerging SOI applications; 2009.

4. Chen CL, Chen CK, Yost DR, Knecht JM, Wyatt, PW, Burns JA, Warner K, Gouker PM, Healey P, Wheeler B, Keast CL. Wafer-scale 3D integration of silicon-on-insulator RF amplifiers. IEEE Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems; 2009.
5. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st ed., Wiley-IEEE Press, USA; 2006.
6. Geng H. Semiconductor manufacturing handbook. 1st ed., McGraw-Hill Education, USA; 2005.
7. Doering R, Nishi Y. Handbook of semiconductor manufacturing technology. 2nd ed., CRC Press, USA; 2007.
8. Wafer Breakage Due to. The Cutting Edge Technical Newsletter; 2008.
9. Combs E. The back-end process: Step 3 - Wafer; 2002.
10. Sumagpang A, Gomez FR. Line stressing critical processes optimization of scalable package passive device for successful production ramp-up. Journal of Engineering Research and Reports. 2018;3(1):1-13.
11. Gomez FR, Mangaoang T. Elimination of ESD events and optimizing waterjet deflash process for reduction of leakage current failures on QFN-mr leadframe devices. Journal of Electrical Engineering, David Publishing Co. 2018;6(4):238-243.

Peer-review history:
The peer review history for this paper can be accessed here:
http://www.sdiarticle3.com/review-history/49689