Applied Artificial Intelligence

An International Journal

ISSN: (Print) (Online) Journal homepage: https://www.tandfonline.com/loi/uaai20

Optimal Sizing of Recycling Folded Cascode Amplifier for Low Frequency Applications Using New Hybrid Swarm Intelligence-Based Technique

Naushad Manzoor Laskar, Koushik Guha, Sourav Nath, K.L. Baishnab & P.K. Paul

To cite this article: Naushad Manzoor Laskar, Koushik Guha, Sourav Nath, K.L. Baishnab & P.K. Paul (2020) Optimal Sizing of Recycling Folded Cascode Amplifier for Low Frequency Applications Using New Hybrid Swarm Intelligence-Based Technique, Applied Artificial Intelligence, 34:13, 994-1010, DOI: 10.1080/08839514.2020.1795786

To link to this article: https://doi.org/10.1080/08839514.2020.1795786

APPLIED ARTIFICIAL INTELLIGENCE
2020, VOL. 34, NO. 13, 994–1010
https://doi.org/10.1080/08839514.2020.1795786

Taylor & Francis
Taylor & Francis Group

Optimal Sizing of Recycling Folded Cascode Amplifier for Low Frequency Applications Using New Hybrid Swarm Intelligence-Based Technique

Naushad Manzoor Laskar, Koushik Guha, Sourav Nath, K.L. Baishnab, and P.K. Paul

Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, India

ABSTRACT

A new efficient design approach for sizing a high performance analog amplifier circuit namely the Recycling Folded Cascode (RFC) amplifier is presented. A RFC amplifier is an enhanced version of the conventional folded cascode amplifier and achieves better slew rate, gain, bandwidth, offset etc. for same area and power budget. Low frequency amplifiers such as bio-medical or neural have a demanding requirement of low area, low power and low noise apart from meeting other optimal design specifications which have inherent trade-off amongst themselves. As a result, manual sizing becomes a computationally inefficient approach. Thus, swarm based optimization techniques have been employed to efficiently determine the optimal sizing for the RFC amplifier such that the area is minimized while meeting all the optimal design specifications considering the constraints. A new hybrid whale particle swarm optimization (HWPSO) algorithm is employed which takes advantage of the good qualities of both the whale algorithm and the PSO algorithm to optimize the area with less computational complexity. Simulations and statistical analysis have been performed and comparisons with other state of art algorithms reveals that HWPSO-based approach achieves a minimum circuit area of 21 μm^2 with a mean Friedman's statistical rank of 2.05 while meeting optimal design specifications for low frequency systems. Finally, validation with circuit design tool Cadence Virtuoso is done and pre as well as post layout analysis have been performed which further illustrated a close agreement with algorithmic results.

Introduction

The design of high performance biomedical or brain-machine front end involves processing of very low amplitude signals (few μV to mV) which lie in the very low frequency range of 100 Hz to few KHz (<20 KHz) (Du and Odame 2013; Wattanapanitch, Fee, and Sarpeshkar 2007). An amplifier is the first major block in these systems and has to be efficiently designed to meet the need of low power and low noise, including other major design specifications

CONTACT Naushad Manzoor Laskar naushad.0015@gmail.com Department of Electronics and Communication Engineering, National Institute of Technology, Silchar, India

for optimal performance. Additionally, an important objective in the design is achieving the required specifications using a minimum circuit area. This is because biomedical or brain-machine interfaces are mostly implanted on human body where only a small area would be available for designing the entire system. For minimizing the circuit area, the transistor dimensions have to be minimized. However, all the major design specifications i.e. Gain, Noise, and CMRR etc. are dependent on the different transistors dimensions, which cannot be arbitrarily minimized, else they would not be able to meet the minimum required specifications for use in the system (Laskar et al. 2017). In addition to this, all the design specifications also have a trade-off amongst themselves. This makes the process of manual sizing of transistors an even difficult and computationally inefficient process (Puhan, Burmen, and Tuma 2003). As a result, optimization algorithms can be employed to achieve the aforementioned objective of minimum area while meeting all the design specifications, which can be formulated as design constraints (De et al. 2015). Among the various classes of optimization algorithms, nature inspired and swarm-based algorithms have been preferred by researchers over the years mainly because of their simplicity, derivative free nature and less computational complexity (Holland 1992; Rao 2009).

Swarm-based algorithms are based on food searching mechanisms of birds or animals and have been employed by many researchers over the years for circuit sizing of various analog circuits to minimize the area (Fakhfakh et al. 2010; Paul et al. 2015; Vural and Yildirim 2011). The first application of any swarm-based algorithm analog circuit sizing was proposed by Vural and Yildirim (2011) where a conventional PSO was employed for area minimization of a differential amplifier and an OpAmp. In recent times, De et al. (2017), De et al. (2018) have employed better and more improved variants of PSO and other algorithms in analog circuit sizing of the previously mentioned circuits. The analog circuit sizing of Folded Cascode OpAmp was proposed by Paul et al. (2015) by using the Human behavior-based PSO. In most recent times, modified hybrid variants of PSO have been employed to design a two stage OpAmp with robust bias circuit (De et al. 2018). One major difference in it is the use of noise as a design criteria which have been ignored prior to it. In none of the reported works, the circuit sizing problem has been performed for amplifiers in neural frequency range. Also, none of the reported works have considered optimizing the RFC circuit, which has better slew rate, gain, bandwidth, offset etc. than a conventional folded cascode amplifier for same area and power budget (Assad and Martine 2009). Thus, the proposed work involves minimizing the circuit area of a RFC amplifier for meeting the design specifications of low frequency applications, which is a major contribution of this work.

Furthermore, from the literature, it is revealed that many researchers have used the PSO (Kennedy and Eberhart 1995) and its variants in optimization of

amplifiers. However, PSO suffers from stagnation effect and thus many variants of it have been proposed (Chen et al. 2013; Liu et al. 2014). In this work, a new Hybrid Whale Particle Swarm Optimization Algorithm (HWPSO) (Laskar et al. 2018) has been employed in minimizing the area of RFC amplifier. HWPSO has been reported to perform efficiently in case of benchmark mathematical as well as electronics design problems with good computational efficiency and better approximation to global optima than other state of art algorithms (Laskar et al. 2018). The use of this HWPSO algorithm in optimal circuit sizing is another contribution of this work. Simulations have been performed and comparison with other state of art algorithms (Kennedy and Eberhart 1995; Price et al. 1995; Zhang and Xie 2003; Mirjalili and Lewis 2016; Mirjalili 2016; Mirjalili et al. 2017) have been performed based on simulations and using statistical tests (Derrac et al. 2011). The results reveal that HWPSO outperforms most of the state of art algorithms by achieving a minimum area of 21 μm^2 and with a better Friedman's rank of 2.05. Further validation in Cadence circuit design tool has been performed using 180 nm technology and pre-layout as well as post-layout analysis have been done. The results are in close agreement with algorithmic results thereby indicating the effectiveness of the approach.

The remainder of the paper is organized as follows. In section 2, the problem formulation for the RFC Circuit is presented. In Section 3, the HWPSO algorithm is discussed. Section 4 presents the results and discussion and finally in Section 5, conclusions are drawn.

Problem Formulation

The RFC Amplifier is shown in Figure 1. It is a modified version of the conventional folded cascode amplifier (Assad and Martine 2009) and uses the current recycling concept by utilizing previously idle devices in the signal path. This is achieved by splitting the sink transistors M3 and M4 in the ratio of K:1, where K is current gain factor. As a result, gain, slew rate etc. are considerably improved. Additionally, for improved matching i.e. to reduce systematic offset two new transistors M11 and M12 as shown in Figure 1. In the circuit, instead of NMOS-based drivers, PMOS-based drivers are better as they offer lower flicker noise (Laskar et al. 2017) Flicker noise is dominant in low frequency and has to be low for minimum noise in low frequency systems (Du and Odame 2013). Thus, in this work, the amplifier design involves PMOS based drivers. A more detailed description on the working of this circuit can be studied from Assad and Martine (2009). The total transistors in this circuit is 12 and thus the objective function and hence the problem statement are defined from Eqn. (1) to Eqn. (14). The design vector for the problem is shown in Eqn. (15). The design specifications is shown in Table 1, and the technology constants are the same as shown in Table 2. The channel lengths

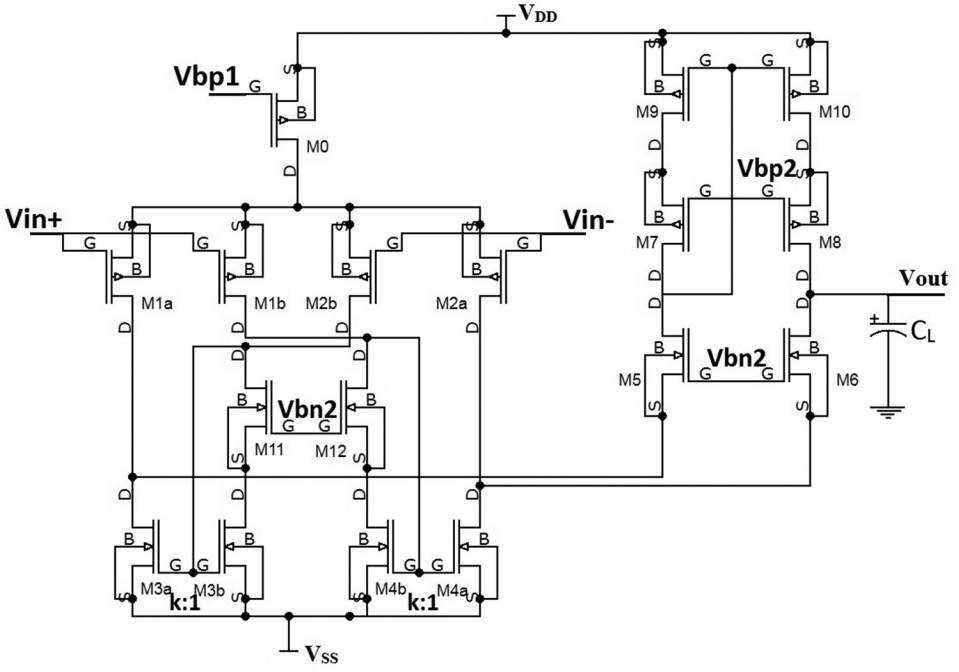

Figure 1. Schematic of RFC OpAmp.

Table 1. Design specifications for use in low frequency systems.

Design Criteria	Specifications
Slew Rate (SR) (V/μs)	≥10
Load Capacitance, C_L (pF)	≥15
Voltage Gain, A_v (dB)	>40
Unity Gain Bandwidth, UGB (MHz)	≥2
Minimum ICMR,$V_{CM(min)}$ (V)	≥-1.6
Maximum ICMR,$V_{CM(max)}$ (V)	≤1.6
CMRR (dB)	> 60
PSRR (dB)	> 60
Power Dissipation, P (μW)	≤7
$V_{out(min)}$ (V)	≥-1.8
$V_{out(max)}$ (V)	≤1.8
Input Referred Noise, S_n (f) (V/√Hz)	≤500 n

for different transistors used are: L = 1 μm (for M1a,M1b,M2a,M2b, M6 and M7), L = 1.25 μm (for M3,M4a,M4b,M5a,M5b), L = 1.5 μm (for M8,M9,M10, M11) and L = 0.5 μm (for M12 and M13). The problem is thus a 7 dimensional problem and hence solved for minimum circuit are subjected to optimal specifications to be met for use in low frequency applications.

$$Minimize\ CF = \sum_{k=0}^{12} W_k L_k \tag{1}$$

Table 2. Values of other technology constants used.

Specification	Values used
V_{DD} (V)	1.8
V_{SS} (V)	−1.8
V_{tp} (V)	−0.42
V_{tn} (V)	0.42
K_n (μA/V^2)	355
K_p (μA/V^2)	75
A_{VTHN}	5 nm
A_{VTHP}	5.49 nm
Technology Node	180 nm
λ_n	0.04
λ_p	0.05

Subjected to

$$I_0 = \frac{(SR)C_L}{K} \tag{2}$$

$$\left(\frac{W}{L}\right)_{4a} = \frac{2I_{4a}}{K_n {V_{DS4a}}^2} = \left(\frac{W}{L}\right)_{3a} \tag{3}$$

$$\left(\frac{W}{L}\right)_{6} = \frac{2I_6}{K_n {V_{DS6}}^2} = \left(\frac{W}{L}\right)_{5} \tag{4}$$

Where RJMC_A_1795910

$$\left(\frac{W}{L}\right)_{10} = \frac{2I_{10}}{K_P {V_{SD10}}^2} \tag{5}$$

$$\left(\frac{W}{L}\right)_{8} = \frac{2I_8}{K_P {V_{SD8}}^2} \tag{6}$$

Where $V_{SD8}(sat) = V_{SD10}(sat) = \frac{V_{DD} - V_{out}(max)}{2}$

$$\left(\frac{W}{L}\right)_{1a} = \left(\frac{W}{L}\right)_{2a} = \left(\frac{W}{L}\right)_{1b} = \left(\frac{W}{L}\right)_{2b} = \frac{g_{m1}^2}{\frac{K_p 2I_3}{K+1}} = \frac{UGB^2 {C_L}^2}{\frac{K_p 2I_3}{K+1}} \tag{7}$$

$$\left(\frac{W}{L}\right)_{0} = \frac{2I_0}{K_p\left[V_{DD} - V_{CM}(max) - \sqrt{\frac{2I_3}{K_p\left(\frac{W}{L}\right)_{1a}}} - V_{tp}\right]^2} \tag{8}$$

$$\left(\frac{W}{L}\right)_{11} = \left(\frac{W}{L}\right)_{12} = \frac{\left(\frac{W}{L}\right)_6}{2} \tag{9}$$

$$\left(\frac{W}{L}\right)_{4b} = \frac{\left(\frac{W}{L}\right)_{4a}}{K}; \left(\frac{W}{L}\right)_{5b} = \frac{\left(\frac{W}{L}\right)_{5b}}{K} \tag{10}$$

$$\left(\frac{W}{L}\right)_{4a} = \frac{2I_{4a}}{K_n\left[V_{CM}(min) - V_{SS} + V_{tp}\right]^2} = \left(\frac{W}{L}\right)_{3a} \tag{11}$$

$$A_v = g_{m1a}(1+K)g_{m6}r_{06}(r_{02a}||r_{04a})||g_{m6}r_{08}r_{010} \tag{12}$$

$$P_{diss} = (V_{DD} + |V_{SS}|)(I_0 + I_9 + I_{10}) \tag{13}$$

$$S_n(f) = \frac{8KT}{3g_{m1}}\left[\frac{5}{4} + \frac{3g_{m3}}{g_{m1}} + \frac{g_{m9}}{4g_{m1}}\right. \tag{14}$$

$$X_{RFC} = \left[SR, A_v, UGB, V_{CM(m)}, V_{CM(max)}, S_n(f), P_{diss}\right] \tag{15}$$

The Hybrid Whale Particle Swarm Optimization Algorithm (HWPSO)

It is a hybrid swarm based meta-heuristic algorithm, proposed by Laskar et al. (2018), considering the positive aspects of two popular swarm based algorithm PSO (Kennedy and Eberhart 1995) and WOA (Mirjalili and Lewis 2016), which results in a better and computationally efficient hybrid algorithm. PSO is characterized by two parameters: position and velocity. The optimal solution is given by the position of the global best particle. In PSO, the velocity and position are updated during every iteration as per Eqn. (16) and Eqn. (17) respectively. However, it has been reported to be suffering from stagnation effect (Chen et al. 2013; Liu et al. 2014). So, to overcome this, it has been hybridized with a Whale Optimization Algorithm (WOA) (Mirjalili and Lewis 2016), which modifies the search mechanism of PSO in such a way that after initialization of position of particles, the WOA search principles are employed, which fine tunes the solution obtained by PSO during the exploration phase (Laskar et al. 2018). This is achieved by the concept of iterative hybridization, where WOA is executed in a secondary iterations within the primary PSO iterations. The reason WOA is employed is because it reports a very good ability of exploration, which enables it to reach global optima efficiently. This concept has been termed as 'Forced' Whale and is implemented using Eqn. (18) and Eqn. (19). However, as WOA has been reported to have poor exploitation ability which leads to poor convergence speed, which on the other hand is a positive aspect in PSO.

Thus, to take advantage of it, the implementation of WOA is terminated in exploitation phase, which is performed solely using PSO. This is achieved by making the WOA secondary iterations dynamically decrease with increase in number of PSO's primary iterations using Eqn. (20). This phenomenon is

called 'Capping' phenomenon. The use of both these techniques results in avoiding of stagnation effect with a good convergence speed, which most of the state of art algorithms cannot achieve without trade-off. The computational complexity of the algorithm is also better than other state of art hybrid approaches (Ranjini and Murugan 2017; Zhang and Xie 2003) and is given by $O(K^2Td)$, where K is the primary iterations, T is the number of particles and 'd' is the dimension of the problem. A more detailed description regarding the working of HWPSO with the search mechanism can be studied from Laskar et al. (2018). The flowchart for the HWPSO for use in RFC area minimization is shown in Figure 2.

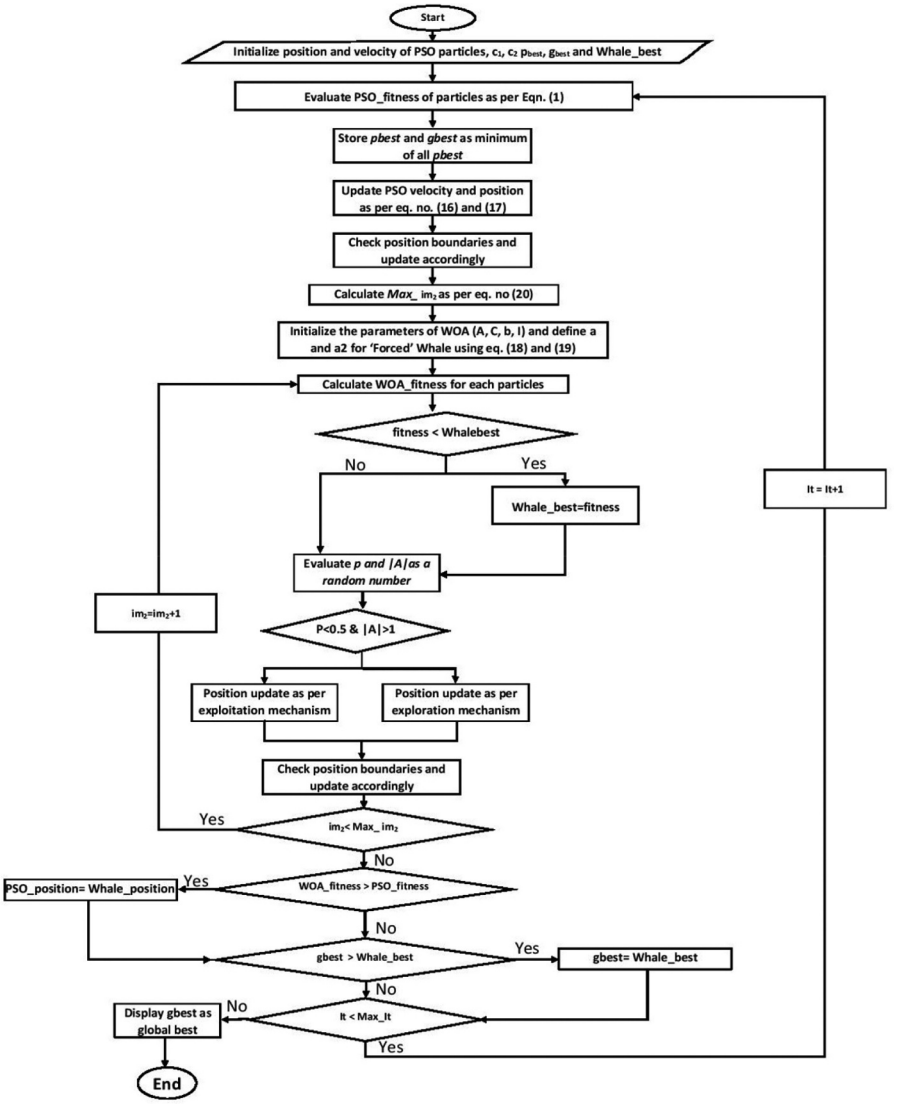

Figure 2. Flowchart of HWPSO algorithm.

$$v_{id}^{k+1} = w.v_{id}^{k} + c_1.rand_1.\left(P_{bestid} - x_{id}^{k}\right) + c_2.rand_2.\left(G_{best} - x_{id}^{k}\right) \tag{16}$$

$$x_{id}^{k+1} = x_{id}^{k} + v_{id}^{k+1} \tag{17}$$

where, c_1 and c_2 are acceleration co-efficient, P_{best} is the local best position which gets updated every iteration, whereas G_{best} is the global best position and w is the damping factor.

$$a = 2 - \left[it.\left(\frac{2}{im_2}\right)\right] \tag{18}$$

$$a_2 = -1 + [it.\left(\frac{-1}{im_2}\right) \tag{19}$$

$$im_2 = [A.(it) + C] \tag{20}$$

Where, 'it' represents primary iteration and im_2 is maximum secondary iteration for WOA (secondary iteration), 'A' and 'C' are constants, which are assigned values based on shape and modes of objective function.

Results and Discussions

HWPSO is utilized in designing a RFC amplifier for low frequency applications such that its circuit area as defined by cost function in Eqn. (1) is minimized and also the constraints defined by Eqn. (2) to Eqn. (14) and Table 1 are met. Additionally, $1 \leq W_k/L_k \leq 100$ has to be met for each of the MOS transistors. A population size of 50 has been considered and this a 50*7 population matrix is formed while solving the problem. A maximum iterations of 100 is chosen and more than 20 independent runs are performed to record the best, worst, mean and standard deviation obtained by HWPSO as well as all the algorithms mentioned previously in Section 1 (Kennedy and Eberhart 1995; Storn et al. 1997; Zhang and Xie 2003; Mirjalili and Lewis 2016; Mirjalili 2016; Mirjalili et al. 2017). Thus, a total of around 2500 function evaluations has been made before recording the optimal data. The results are indicated in Tables 3 to 5, respectively. Table 5 illustrates that for the current problem although the best value for DA, HBPSO and WOA are same as HWPSO but their standard deviation (SD) is more than HWPSO, which signifies that HWPSO is more consistent for a long run. The statistical significance of the algorithms is again tested for this problem by performing Friedman's test using fitness values of the cost function obtained during every run. It signifies the statistical difference in the results of two algorithms (Derrac et al. 2011). The results are indicated in Table 6, which shows that HWPSO performs the best among all the state of art algorithms used having a mean rank of 2.05 for

Table 3. Comparative analysis of the best results obtained using HWPSO and other algorithms after 20 independent runs.

Design Criteria	PSO	DE	DEPSO	HBPSO	DA	WOA	SSA	HWPSO
Slew Rate (V/s)	10	2.41	2.41	15.07	15.07	15.07	2.41	15.07
Unity Gain Bandwidth (MHz)	3.5	3.5	3.5	0.55	0.55	0.55	3.5	0.55
Voltage Gain (dB)	54.32	54.32	54.32	56.11	56.11	56.11	54.32	56.11
$V_{CM(min)}$ (V)	−0.294	−0.2937	−0.2937	−1.4	−1.4	−1.4	−0.294	−1.4
$V_{CM(max)}$(V)	1.4874	1.4874	1.4874	1.11	1.11	1.11	1.4874	1.11
Power Dissipation (μW)	3.6907	3.69072	3.69072	6.106	6.106	6.106	3.6907	6.106
CMRR (dB)	83.68	83.68	83.68	74.48	74.48	74.48	83.68	74.48
PSRR (dB)	57.19	57.19	57.19	58.50	58.50	58.50	57.19	58.50
Input Noise (μV/√Hz)	0.97	0.97	0.97	0.89	0.89	0.89	0.97	0.89
Cut off frequency (KHz)	6.76	6.76	6.76	0.851	0.851	0.851	6.76	0.851
Total Area (m^2)	2.19e-10	2.19e-10	2.19e-10	2.12e-11	2.12e-11	2.12e-11	2.19e-10	2.12e- 11

Table 4. Optimal design parameters corresponding to best results obtained using HWPSO and other algorithms.

Design Parameters	PSO	DE	DEPSO	HBPSO	DA	WOA	SSA	HWPSO
I_0 (μA)	33.3	33.3	33.3	50.53	50.53	50.53	33.3	50.53
W_{1a}/L_1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
W_{1b}/L_1	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
W_{2b}/L_2	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
W_{2b}/L_2	1/1	1/1	1/1	1/1	1/1	1/1	1/1	1/1
W_3/L_3	1.25/1.25	0.2664/1.25	0.2664/1.25	0.5435/0.5	20.89/0.5	0.5435/0.5	1.25/1.25	0.5435/0.5
W_{4a}/L_4	7.8247/1.25	7.8247/1.25	7.8247/1.25	1.25/1.25	1.25/1.25	1.25/1.25	7.8247/1.25	1.25/1.25
W_{4b}/L_4	2.6082/1.25	2.6082/1.25	2.6082/1.25	0.4167/1.25	0.4167/1.25	0.4167/1.25	2.6082/1.25	0.4167/1.25
W_{5a}/L_5	7.8247/1.25	7.8247/1.25	7.8247/1.25	1.25/1.25	1.25/1.25	1.25/1.25	7.8247/1.25	1.25/1.25
W_{5b}/L_5	2.6082/1.25	2.6082/1.25	2.6082/1.25	0.4167/1.25	0.4167/1.25	0.4167/1.25	2.6082/1.25	0.4167/1.25
W_6/L_6	4.1732/1	4.1732/1	4.1732/1	1/1	1/1	1/1	4.1732/1	1/1
W_7/L_7	4.1732/1	4.1732/1	4.1732/1	1/1	1/1	1/1	4.1732/1	1/1
W_8/L_8	29.62/1.5	29.62/1.5	29.62/1.5	1.5/1.5	1.5/1.5	1.5/1.5	29.62/1.5	1.5/1.5
W_9/L_9	29.62/1.5	29.62/1.5	29.62/1.5	1.5/1.5	1.5/1.5	1.5/1.5	29.62/1.5	1.5/1.5
W_{10}/L_{10}	29.62/1.5	29.62/1.5	29.62/1.5	1.5/1.5	1.5/1.5	1.5/1.5	29.62/1.5	1.5/1.5
W_{11}/L_{11}	29.62/1.5	29.62/1.5	29.62/1.5	1.5/1.5	1.5/1.5	1.5/1.5	29.62/1.5	1.5/1.5
W_{12}/L_{12}	2.0866/0.5	2.0866/0.5	2.0866/0.5	0.5/0.5	0.5/0.5	0.5/0.5	2.0866/0.5	0.5/0.5
W_{13}/L_{13}	2.0866/0.5	2.0866/0.5	2.0866/0.5	0.5/0.5	0.5/0.5	0.5/0.5	2.0866/0.5	0.5/0.5

Table 5. Comparative results of algorithms in terms of best, worst, mean and standard deviation after more than 20 independent runs.

Optimum Circuit Area (m^2)	PSO	DE	DEPSO	HBPSO	DA	WOA	SSA	HWPSO
Best	2.19e-10	2.19e-10	2.19e-10	2.12e-11	2.12e-11	2.12e-11	2.19e-10	2.12e-11
Worst	2.19e-10	2.19e-10	2.19e-10	4.86e-11	4.86e-11	4.57e-11	2.19e-10	4.57e-11
Mean	2.19e-10	2.19e-10	2.19e-10	3.89e-11	3.89e-11	3.75e-11	2.19e-10	3.34e-11
SD	0	0	0	1.38e-11	1.38e-11	1.35e-11	0	1.34e-11

a 5% level of significance. The post-hoc analysis is then performed for testing whether the difference between HWPSO's samples and other algorithms samples are statistically different or not using Mann Whitney U test. As

Table 6. Friedman's test result considering minimum area for 20 independent runs.

Algorithm	Mean Rank	Rank
PSO	6.4500	4
DE	6.6500	5
DA	2.9000	3
WOA	2.1500	2
HWPSO	2.0500	1

Table 7. Mann Whitney U test result.

HWPSO vs.	p-value	U value	HWPSO U value
PSO	0.0000108	0	100
DE	0.0000108	0	100
DA	0.10	28.5	71.5
WOA	0.21	33.5	66.5

HWPSO is ranked 1 in Friedman's test, it becomes the controlling algorithm in Mann Whitney U test and the statistical difference of its results with other algorithms is tested. The results are shown in Table 7. From Table 7, the *p*-values and U values of the results indicate that the results are statistically significant. However, in case of WOA and DA, the *p* values are too large to reject the null hypothesis that the two samples are statistically different considering a 5% level of significance. But, the U values of HWPSO are better than the U values of both DA and WOA, from which it can be said that HWPSO results are statistically better. Based on the comparative results and analysis with other state of art algorithms, the effectiveness of HWPSO is illustrated in designing a high performance RFC Amplifier for low frequency with minimum (best) circuit area of 21 μm^2. The convergence plot shown in Figure 3 (a) further indicates that HWPSO has a faster convergence than the other state of art algorithms in terms of number of iterations taken to converge in achieving a minimum area. The boxplot shown in Figure 3 (b) indicates that HWPSO performs consistently for more than 2000 function evaluations with the optimum values lying close to each other and with a low standard deviation. The plot is in accordance with the data shown in Table 5.

The results in Table 3 indicate that HWPSO-based design is able to achieve the highest gain of 56.11 dB with a cutoff frequency of 0.851 KHz, which is suitable for use in recording local field potentials of Neural Amplifiers and also in biomedical applications such as ECG and EEG recordings. Furthermore, the input referred noise is significantly better in comparison to other state of art algorithms with values of 0.89 $\mu V/\sqrt{Hz}$. This is mainly due to the values of W_{4a}/L_4 to W_{5b}/L_5 obtained using the algorithm. However, this results in a minor trade-off with a comparatively higher power dissipation of 6.106 μW resulting from increased I_0 as compared to a PSO- or DEPSO-based design as indicated in Figure 4. Validation of the HWPSO results have been performed by redesigning a RFC Amplifier corresponding to the best results in Cadence

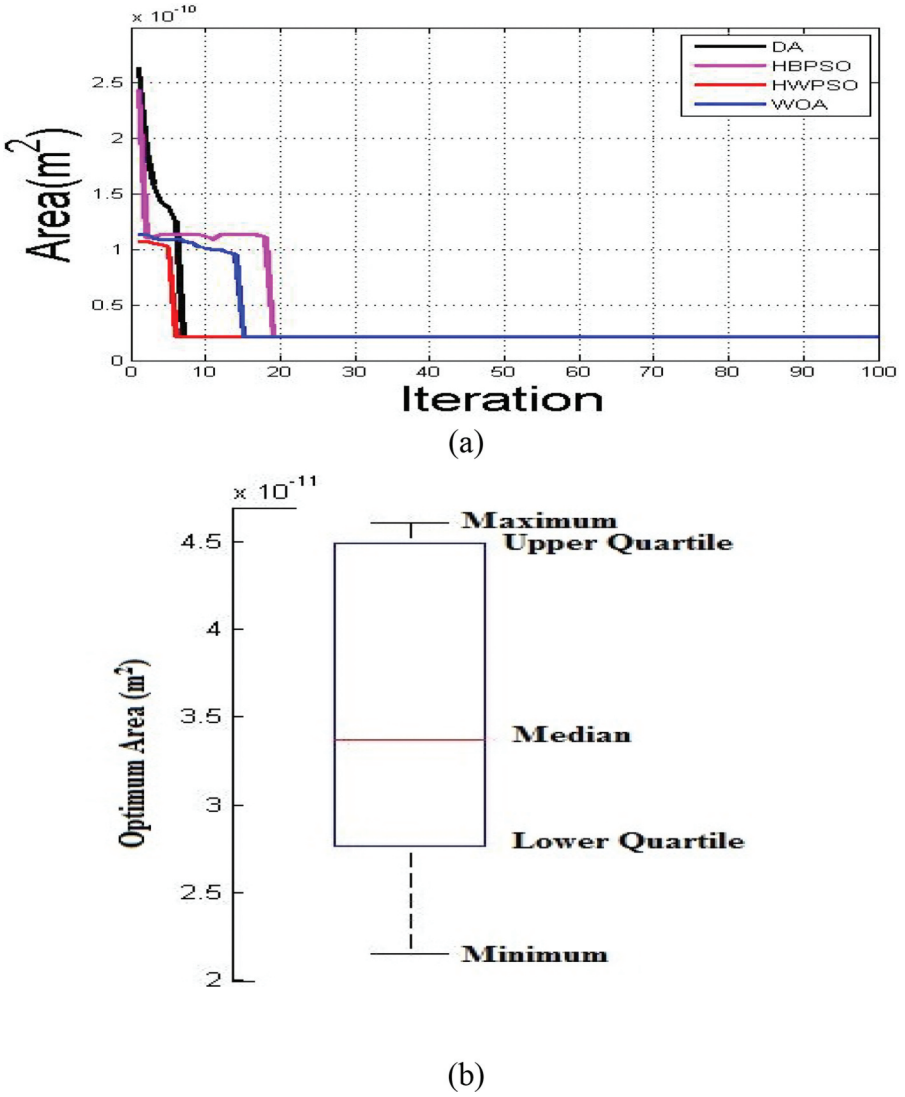

Figure 3. (a) Comparative analysis of the convergence plot (b) Box plot for HWPSO for the problem.

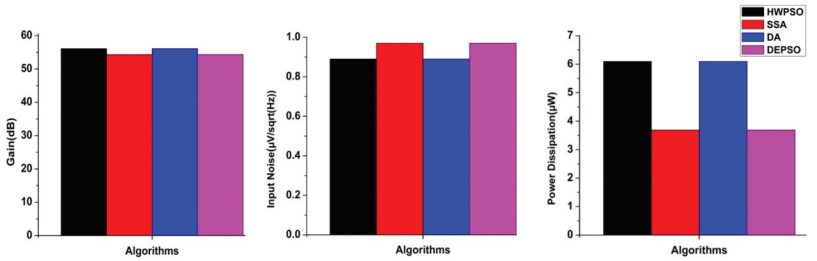

Figure 4. Comparison of various specifications for the algorithms.

Virtuoso using 180 nm technology parameters and performing pre and post layout simulations. The results are shown in Figures 5-10, which are in close agreement with algorithmic results with very small deviation in the range of 0.13 to 1.9% for different design parameters as indicated in Table 8. The layout of the RFC amplifier circuit is shown in Figure 11. The deviation can be attributed to parasitic effects and certain higher order effects neglected in the modeling of the circuit.

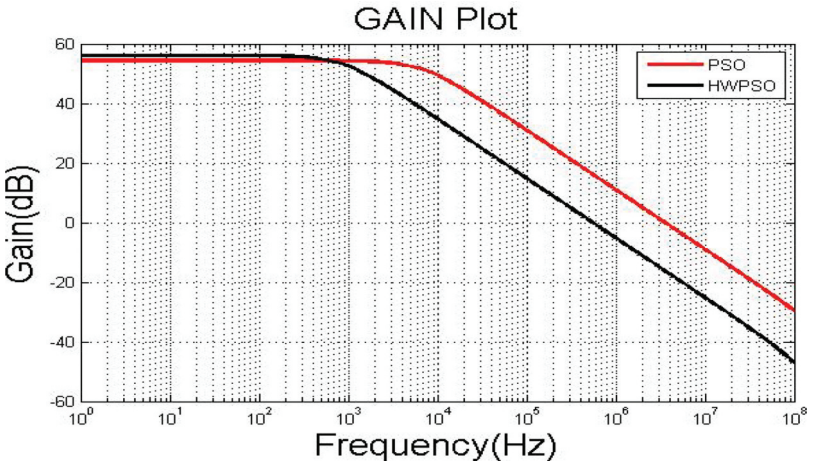

Figure 5. Cadence virtuoso simulated gain plot.

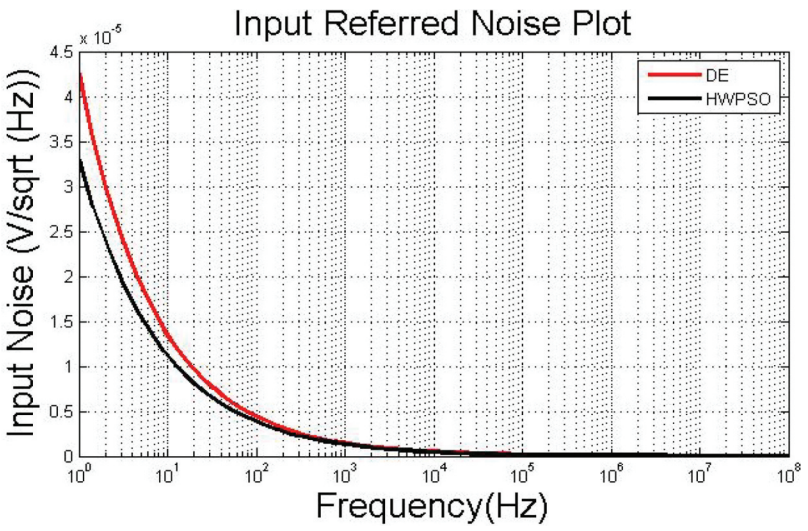

Figure 6. Cadence virtuoso simulated input referred noise plot.

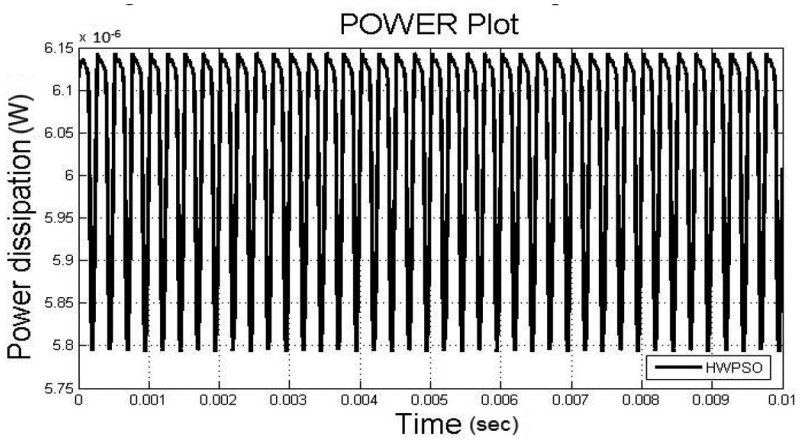

Figure 7. Cadence virtuoso simulated power dissipation plot for HWPSO algorithm.

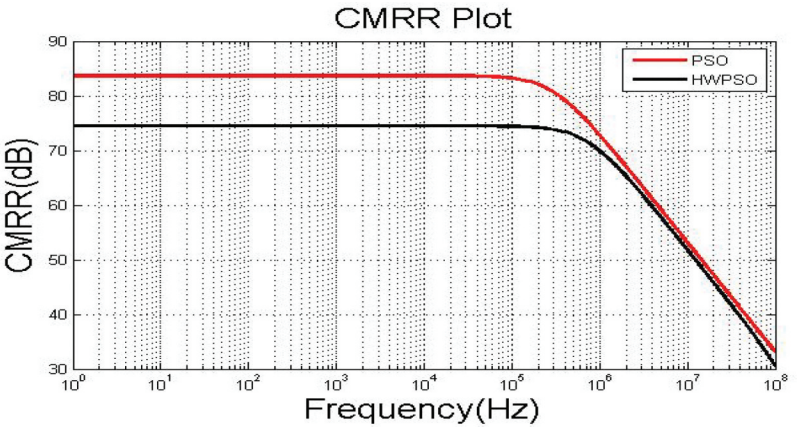

Figure 8. Cadence virtuoso simulated CMRR plot for HWPSO algorithm.

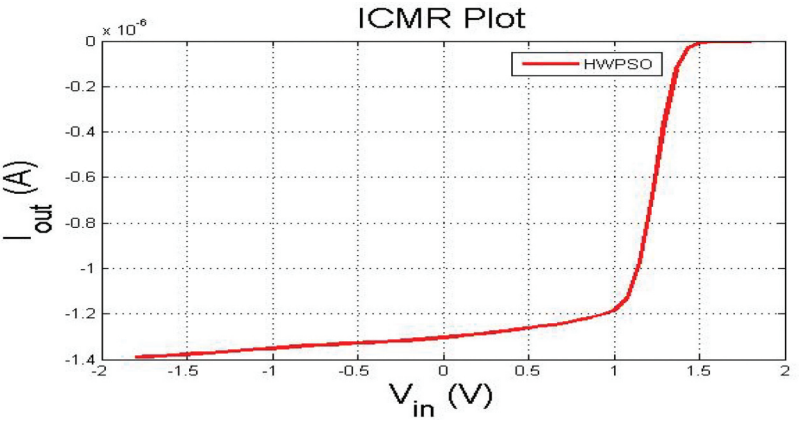

Figure 9. Cadence virtuoso simulated ICMR plot for HWPSO algorithm.

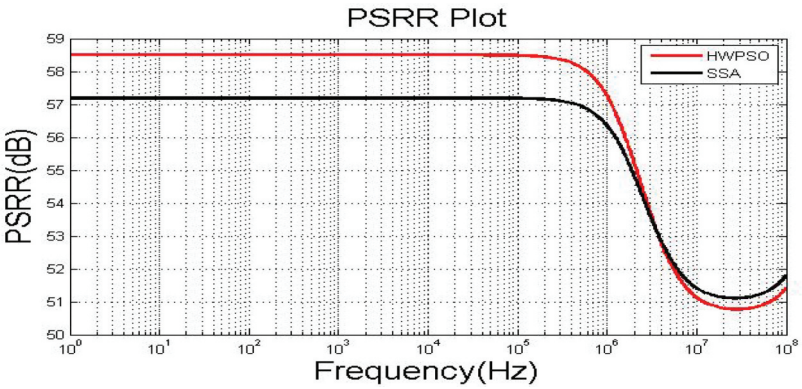

Figure 10. Cadence virtuoso simulated PSRR plot for HWPSO algorithm.

Table 8. Validation results for HWPSO and % deviation.

Design Criteria	HWPSO based optimization results	Cadence Virtuoso validation results for HWPSO (Pre-layout)	Cadence Virtuoso validation results for HWPSO (Post-layout)	% deviation (Pre-Post)
Slew Rate (V/μs)	15.07	15.1	15.05	0.19–0.13
UGB(MHz)	0.55	0.556	0.553	1.09–0.54
Gain(dB)	56.11	55.9	55.6	0.37–0.9
$V_{CM(min)}$ (V)	−1.4	−1.393	−1.390	0.5–0.71
$V_{CM(max)}$ (V)	1.11	1.116	1.114	0.54–0.36
Power dissipation (μW)	6.106	6.098	6.092	0.26–0.22
CMRR (dB)	74.48	74.12	74.07	0.48–0.55
PSRR (dB)	58.50	58.9	59.01	0.67–0.87
Input Noise (μV/√Hz)	0.89	0.902	0.905	1.3–1.6

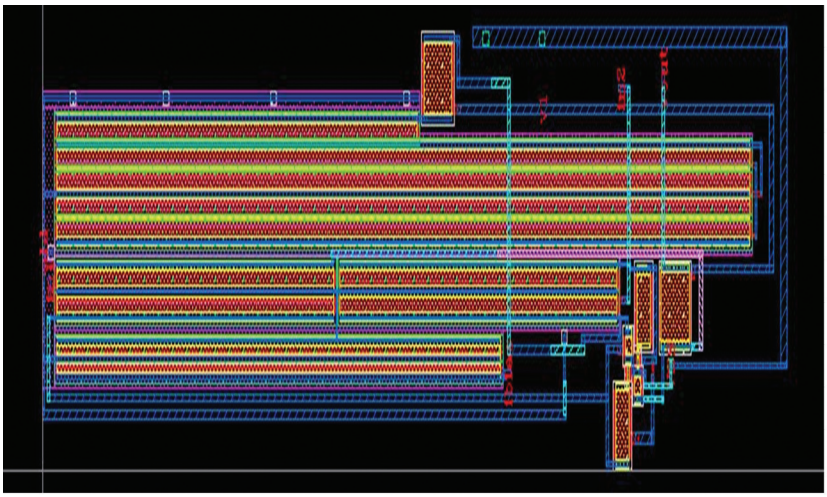

Figure 11. Layout of RFC OpAmp in cadence virtuoso.

Conclusion

In the proposed work, optimal sizing for a CMOS front end RFC amplifier for use in low frequency applications such as biomedical, neural recording etc. has been presented. For this, a new hybrid meta-heuristic algorithm namely Hybrid Whale Particle Swarm Optimization (HWPSO) has been utilized. The proposed algorithm minimizes the circuit area for the amplifier and also determines the optimum values of the design variables within the constraints required for them to be used in low frequency applications. Simulations have been performed for more than 2,000 evaluation of the objective functions in both the cases and the best results are recorded. Statistical analysis and comparison with other state of art algorithms illustrated that outperforms most of the state of art algorithms. Although performance of HWPSO is in par with WOA and DA in terms of minimum circuit area but statistically it performs better and with more consistency. Additionally, it also has a faster convergence speed. Further validation has been performed by redesigning the circuits corresponding to the best results after 20 independent runs in Cadence Virtuoso using 180 nm technology parameters and the results are found to be in close agreement with each other with a deviation of around 1% only, which can be attributed to certain higher order effects neglected during the optimization problem and constraint formulation. A small deviation arising between pre and post layout results of different specifications can be attributed to the parasitic effects which comes in to play after the layout is done. The proposed work can be extended to include offset modeling for the circuit solved for minimum offset, which can be considered as a future enhancement to this work.

Acknowledgments

The authors are highly thankful to the Ministry of Electronics Information Technology (MeitY), Govt. of India and SCL Mohali, for providing necessary grants, EDA Tools and technology files under SMDP-C2SD Project for the smooth functioning of the work.

References

Assad, R. S., and J. S. Martine. 2009. The recycling folded cascode: a general enhancement of the folded cascode amplifier. *IEEE Journal of Solid-state Circuits* 44 (9):2535–42. doi:10.1109/JSSC.2009.2024819.

Chen, W. N., J. Zhang, Y. Lin, N. Chen, Z. H. Zhan, H. Chung, Y. Li, and Y. Hshi. 2013. Particle swarm optimization with an aging leader and challengers. *IEEE Transactions on Evolutionary Computation* 17:241–58. doi:10.1109/TEVC.2011.2173577.

De, B. P., K. B. Maji, D. Chowdhury, R. Kar, D. Mandal, and S. P. Ghoshal 2017. Application of PSO variants for optimal design of two-stage CMOS Op-amp with robust bias circuit.

Lecture Notes on Electrical Engineering, Communication, Devices and Computing, Proceedings of ICCDC, Haldia, WB, India, Springer, 263–72.

De, B. P., K. B. Maji, R. Kar, D. Mandal, and S. P. Ghoshal. 2018. Design of optimal CMOS analog amplifier circuits using a hybrid evolutionary optimization technique. *Journal of Circuits, Systems and Computers* 27 (2):18500–1:23. doi:10.1142/S0218126618500299.

De, B. P., R. Kar, D. Mandal, and S. P. Ghoshal. 2015. Optimal analog active filter design using craziness based particle swarm optimization algorithm. *The International Journal of Numerical Modelling: Electronic Networks, Devices and Fields* 28 (5):593–609. doi:10.1002/jnm.2040.

Derrac, J., S. Garcia, D. Molina, and F. Herrera. 2011. A practical tutorial on the use of nonparametric statistical tests as a methodology for comparing evolutionary and swarm intelligence algorithms. *Swarm and Evolutionary Computation, Elsevier* 1:3–18. doi:10.1016/j.swevo.2011.02.002.

Du, D., and K. M. Odame. 2013. A bandwidth-adaptive preamplifier. *IEEE Journal of Solid-state Circuits* 48 (9):2142–53. doi:10.1109/JSSC.2013.2266869.

Fakhfakh, M.,Y. Cooren, A. Sallem, M. Loulou, P. Siarry. 2010. Analog circuit design optimization through the particle swarm optimization technique. *Analog Integrated Circuits and Signal Processing* 63:71–82. doi:10.1007/s10470-009-9361-3.

Holland, J. H. 1992. Genetic algorithms. *Scientific American* 267:66–72. doi:10.1038/scientificamerican0792-66.

Kennedy, J., and R. C. Eberhart 1995. Particle swarm optimization. Proceedings of the 1995 IEEE International Conference on Neural Networks, IEEE Service Center, Piscataway, NJ.

Laskar, N. M., K. Guha, I. Chattarjee, S. Chanda, K. L. Baishnab, and P. K. Paul. 2018. HWPSO: A new hybrid whale-particle swarm optimization algorithm and its application in electronic design optimization problems. *Applied Intelligence, Springer*. (Available Online). doi:10.1007/s10489-018-1247-6.

Laskar, N. M., S. Nath, S. Chanda, and K. L. Baishnab 2017. A high gain, low power two stage OpAmp using self cascoding technique for low frequency application. IEEE Conference on Devices for Integrated Circuits (DevIC). Kalyani, India.

Liu, H., G. Xu, G. Y. Ding, and Y. B. Sun. 2014. Human behavior based particle swarm optimization. *Hindawi Publishing Corporation, The Scientific World Journal Volume-2014,* 1-14.

Mirjalili, S. 2016. Dragonfly algorithm: A new meta-heuristic optimization technique for solving single-objective, discrete, and multi- objective problems. *Neural Comput & Applications, Springer* 27:1053–73. doi:10.1007/s00521-015-1920-1.

Mirjalili, S., and A. Lewis. 2016. The whale optimization algorithm. *Advances in Engineering Software* 95:51–67. doi:10.1016/j.advengsoft.2016.01.008.

Mirjalili, S., A. H. Gandomi, S. Z. Mirjalili, S. Saremi, H. Faris, and S. M. Mirjalili. 2017. Salp swarm algorithm: A bio-inspired optimizer for engineering design problems. Advances in Engineering Software, vol.114, pp. 163-191, Elsevier.

Paul, P. K., N. M. Laskar, S. Nath, and K. L. Baishnab. 2015. Performance analysis of new swarm intelligence based algorithms in optimizing the design of CMOS folded cascode OPAMP and comparator circuits. *International Journal of Applied Engineering Research* 10 (5):43620–29.

Price, K., and R. Storn 1995. Differential evolution – A simple and efficient adaptive scheme for global optimization over continuous spaces. Technical Report, International Computer Science Institute, Berkley.

Puhan, J., A. Burmen, and T. Tuma. 2003. Analogue integrated circuit sizing with several optimization runs using heuristics for setting initial points. *Canadian Journal of Electrical and Computer Eng.* 28:105–11. doi:10.1109/CJECE.2003.1425097.

Ranjini, S., and S. Murugan. 2017. Memory based hybrid dragonfly algorithm for numerical optimization problems. *Expert Systems with Applications, Elsevier* 83:63–78. doi:10.1016/j.eswa.2017.04.033.

Rao, S. S. 2009. *Engineering optimization theory and practice*. Fourth ed. Hoboken, New Jersey: (John Wiley & Sons Inc.).

Vural, R. A., and T. Yildirim. 2011. Swarm intelligence based sizing methodology for CMOS operational amplifier. *Proceedings of 12th IEEE Symposium on Computational Intelligence and Informatics* 525–28.

Wattanapanitch, W., M. Fee, and S. Sarpeshkar. 2007. An energy efficient micropower neural recording amplifier. *IEEE Transactions on Biomedical Circuits and Systems* 1 (2):136–47. doi:10.1109/TBCAS.2007.907868.

Zhang, W. J., and X. F. Xie. 2003. DEPSO: Hybrid particle swarm with differential evolution operators. *Proceedings of the IEEE International Conference on System, Security and Assurance* 3816–21.